REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Clarify test conditions for V_{DR}, t_{CCDR}, t_{CDR}, and t_R in table I. Add case outline Z. Add CAGE 61772 as source of supply for case outline Z. Update to new boilerplate. Editorial changes throughout. - jdb	97-10-23	Raymond Monnin

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
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APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
93-05-04

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 4K X 8 DUAL PORT STATIC RANDOM ACCESS MEMORY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89764**

SHEET 1 OF 26

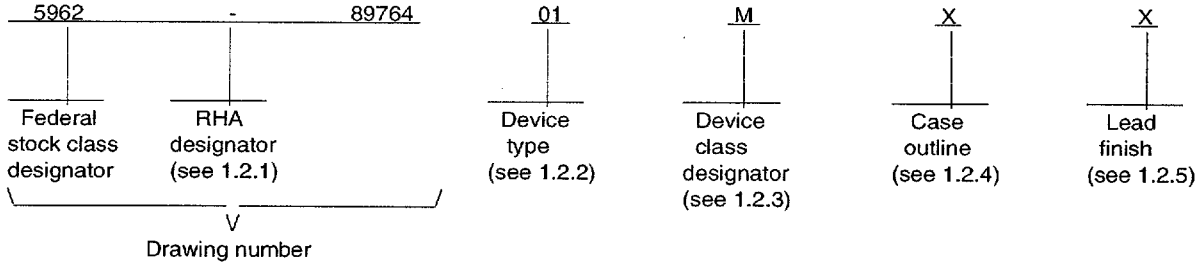
DSCC FORM 2233
APR 97

5962-E270-97

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time	Dynamic operating current
01		4k x 8 dual port CMOS SRAM	70 ns	270 mA
02		4k x 8 dual port CMOS SRAM	70 ns	220 mA
03		4k x 8 dual port CMOS SRAM	55 ns	270 mA
04		4k x 8 dual port CMOS SRAM	55 ns	220 mA
05		4k x 8 dual port CMOS SRAM	45 ns	280 mA
06		4k x 8 dual port CMOS SRAM	45 ns	240 mA
07		4k x 8 dual port CMOS SRAM	35 ns	300 mA
08		4k x 8 dual port CMOS SRAM	35 ns	260 mA

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T48 or CDIP2-T48	48	Dual-in-line package
Y	See figure 1	48	Square chip carrier package
Z	See figure 1	48	Flat pack

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.6.2 herein).

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage	-0.5 V dc to +6.0 V dc
DC output current	-50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	2.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	See MIL-STD-1835
Case outlines Y and Z	6°C/W
Junction temperature (T_J)	+150°C 3/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.2 V dc to 6.0 V dc
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 4/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	5/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.
4/ V_{IL}(min) = -3.0 V dc for pulse width less than 20 ns.
5/ Values will be added when they become available.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional block diagram. The functional block diagram shall be as specified on figure 4.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OH} = 6.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
		V_{IL} = 0.8 V, I_{OH} = 8.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.5	V
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5 V, GND ≤ V_{IN} ≤ V_{CC}	1, 2, 3	02,04, 06,08		5.0	µA
				01,03, 05,07		10	
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}	1, 2, 3	02,04, 06,08		5.0	µA
				01,03, 05,07		10	
Dynamic operating current (both ports active)	I_{CC}	$\overline{CE}$ = V_{IL}, f = f_{MAX} 1/, outputs open	1, 2, 3	01,03		270	mA
				02,04		220	
				05		280	
				06		240	
				07		300	
				08		260	
Standby power supply current (both ports-TTL input levels)	I_{SB1}	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX} 1/	1, 2, 3	01,03, 05		70	mA
				02,04, 06		50	
				07		75	
				08		55	
Standby power supply current (one port-TTL input levels)	I_{SB2}	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX} 1/, active port outputs open	1, 2, 3	01,03		180	mA
				02,04		150	
				05		190	
				06		160	
				07		200	
				08		170	
Full standby power supply current (both ports-CMOS input levels)	I_{SB3}	Both ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2 V, V_{IN} ≥ V_{CC} - 0.2 V or ≤ 0.2 V, f = 0 1/	1, 2, 3	01,03, 05,07		30	mA
				02,04, 06,08		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Full standby power supply current (one port-CMOS input levels)	I_{SB4}	f = f_{MAX} 1/ $\overline{CEL}$ or $\overline{CE}_R \geq V_{CC}$ - 0.2 V, $V_{IN} \geq V_{CC}$ - 0.2 V or $\leq$ 0.2 V, active port outputs open	1, 2, 3	01,03		170	mA
				02,04		140	
				05		180	
				06		150	
				07		190	
				08		160	
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0 V, $\overline{CE} \geq V_{CC}$ - 0.2 V $V_{IN} \geq V_{CC}$ - 0.2 V or $\leq$ 0.2 V	1, 2, 3	02,04, 06,08	2.0		V
Data retention current	t_{CCDR}		1, 2, 3	02,04, 06,08		4.0	mA
Chip deselect to data retention time 2/	t_{CDR}		9, 10, 11	02,04, 06,08	0		ns
Operation recovery time 2/	t_R		9, 10, 11	02,04, 06,08	t_{RC} 3/		ns
Input capacitance	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, see 4.4.1e	4	All		11	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V, f = 1.0 MHz, T_A = +25°C, See 4.4.1e	4	All		11	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			
Read cycle time	t_{RC}	See figures 5 and 6	9, 10, 11	01,02	70		ns
				03,04	55		
				05,06	45		
				07,08	35		
Address access time	t_{AA}		9, 10, 11	01,02		70	ns
				03,04		55	
				05,06		45	
				07,08		35	
Output hold from address change	t_{OH}		9, 10, 11	All	0		ns
Chip enable access time	t_{ACE}		9, 10, 11	01,02		70	ns
				03,04		55	
				05,06		45	
				07,08		35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output enable access time	t_{AOE}	See figures 5 and 6	9, 10, 11	01,02		40	ns
				03,04		30	
				05,06		25	
				07,08		20	
Output low Z time 2/ 4/	t_{LZ}		9, 10, 11	01-06	5		ns
				07,08	0		
Output high Z time 2/ 4/	t_{HZ}		9, 10, 11	01,02		30	ns
				03,04		25	
				05-08		20	
Chip enable to power-up time 2/	t_{PU}		9, 10, 11	All	0		ns
Chip disable to power-down time 2/	t_{PD}		9, 10, 11	All		50	ns
Write cycle time	t_{WC}		9, 10, 11	01,02	70		ns
				03,04	55		
				05,06	45		
				07,08	35		
Chip enable to end of write	t_{EW}		9, 10, 11	01,02	60		ns
				03,04	50		
				05,06	40		
				07,08	30		
Address valid to end of write	t_{AW}		9, 10, 11	01,02	60		ns
				03,04	50		
				05,06	40		
				07,08	30		
Address setup time	t_{AS}		9, 10, 11	All	0		ns
Write pulse width	t_{WP}		9, 10, 11	01,02	60		ns
				03,04	50		
				05,06	40		
				07,08	30		
Write recovery time	t_{WR}		9, 10, 11	All	0		ns

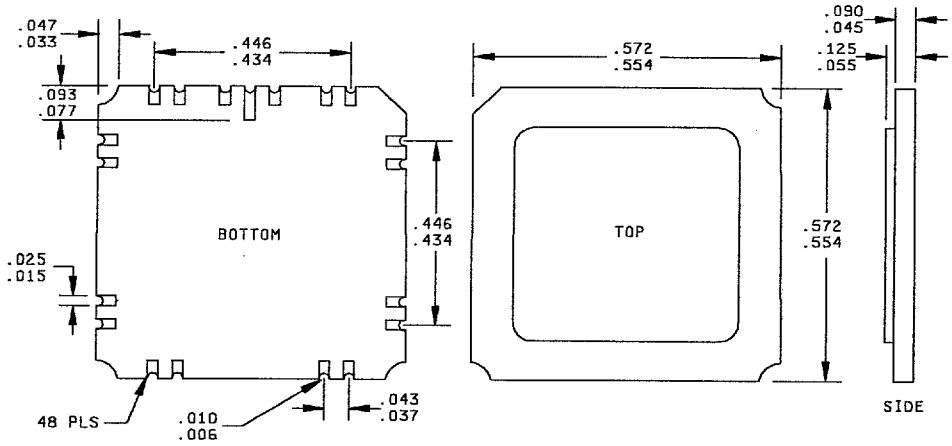
See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data valid to end of write	t_{DW}	See figures 5 and 6	9, 10, 11	01,02	30		ns
				03,04	25		
				05-08	20		
Data hold time 5/	t_{DH}		9, 10, 11	All	3.0		ns
Write enable to output in high Z 2/ 4/	t_{WZ}		9, 10, 11	01,02		30	ns
				03,04		25	
				05-08		20	
Output active from end of write 2/ 4/ 5/	t_{OW}		9, 10, 11	All	3.0		ns
Write pulse to data delay 6/	t_{WDD}		9, 10, 11	01,02		90	ns
				03-06		80	
				07,08		70	
Write data valid to read data delay 6/	t_{DDD}		9, 10, 11	01,02		70	ns
				03,04		65	
				05-08		55	

1/ $f_{max} = 1/t_{RC}$ = All inputs cycling at $f = 1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.
2/ Parameter may not be tested, but shall be guaranteed to the limits specified in Table I.
3/ t_{RC} = Read Cycle Time.
4/ Transition is measured ±500 mV from low or high impedance voltage with load.
5/ The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
6/ Port-to-port delay through RAM cells from writing port to reading port.

Case Y

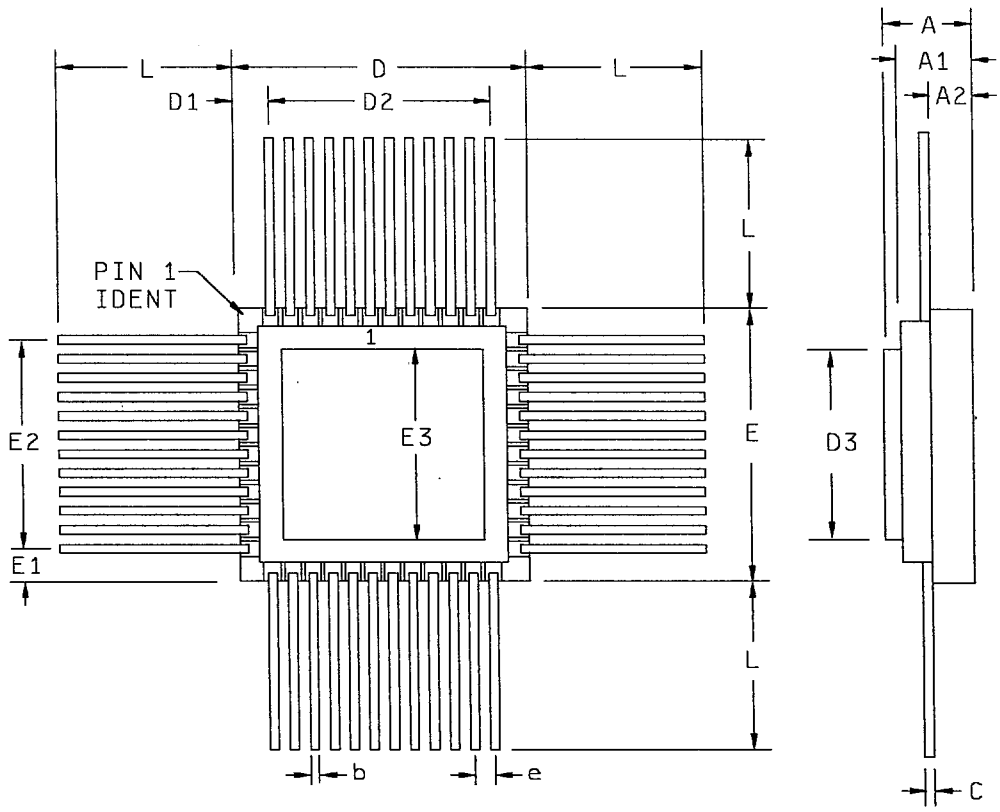


Inches	Millimeters	Inches	Millimeters
.006	0.15	.055	1.40
.010	0.25	.077	1.96
.015	0.38	.090	2.29
.025	0.64	.093	2.36
.033	0.84	.125	3.18
.037	0.94	.434	11.02
.043	1.09	.446	11.33
.045	1.14	.554	14.07
.047	1.19	.572	14.53

Note: Controlling dimensions are inches.

FIGURE 1. Case outlines.

Case Z



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.089	0.108	2.26	2.74
A1	0.079	0.096	2.01	2.44
A2	0.058	0.073	1.47	1.85
b	0.018	0.022	0.46	0.56
C	0.008	0.010	0.20	0.25
D		0.750		19.05
D1	.100 REF		2.54 REF	
D2	.550 BSC		13.97 BSC	
D3	---	0.550	---	13.97

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
e	.050 BSC		1.27 BSC	
E	---	0.75	---	19.05
E1	.100 REF		2.54 REF	
E2	.550 BSC		13.97 BSC	
E3	---	0.550	---	13.97
L	0.350	0.450	8.89	11.43
ND	12			
NE	12			

FIGURE 1. Case outlines - continued.

Device types	ALL	Device types	ALL
Case outlines	X, Y AND Z	Case outlines	X, Y AND Z
Terminal number	Terminal symbol 1/	Terminal number	Terminal symbol 1/
1	$\overline{CE}_L$	25	I/O_{0R}
2	$R/\overline{W}_L$	26	I/O_{1R}
3	A_{11L}	27	I/O_{2R}
4	A_{10L}	28	I/O_{3R}
5	$\overline{OE}_L$	29	I/O_{4R}
6	A_{0L}	30	I/O_{5R}
7	A_{1L}	31	I/O_{6R}
8	A_{2L}	32	I/O_{7R}
9	A_{3L}	33	A_{9R}
10	A_{4L}	34	A_{8R}
11	A_{5L}	35	A_{7R}
12	A_{6L}	36	A_{6R}
13	A_{7L}	37	A_{5R}
14	A_{8L}	38	A_{4R}
15	A_{9L}	39	A_{3R}
16	I/O_{0L}	40	A_{2R}
17	I/O_{1L}	41	A_{1R}
18	I/O_{2L}	42	A_{0R}
19	I/O_{3L}	43	$\overline{OE}_R$
20	I/O_{4L}	44	A_{10R}
21	I/O_{5L}	45	A_{11R}
22	I/O_{6L}	46	$R/\overline{W}_R$
23	I/O_{7L}	47	$\overline{CE}_R$
24	GND	48	V_{CC}

1/ An L suffix on a terminal indicates that it applies to the left port, and an R suffix indicates that it applies to the right port.

FIGURE 2. Terminal connections.

Read/Write Control

Left or Right Port 1/				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Post disabled and in power down mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, power down mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on port written into memory
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

1/ A_{0L}-A_{11L} is not equal to A_{0R}-A_{11R}
H = High
L = Low
X = Don't care
Z = High impedance

FIGURE 3. Truth table.

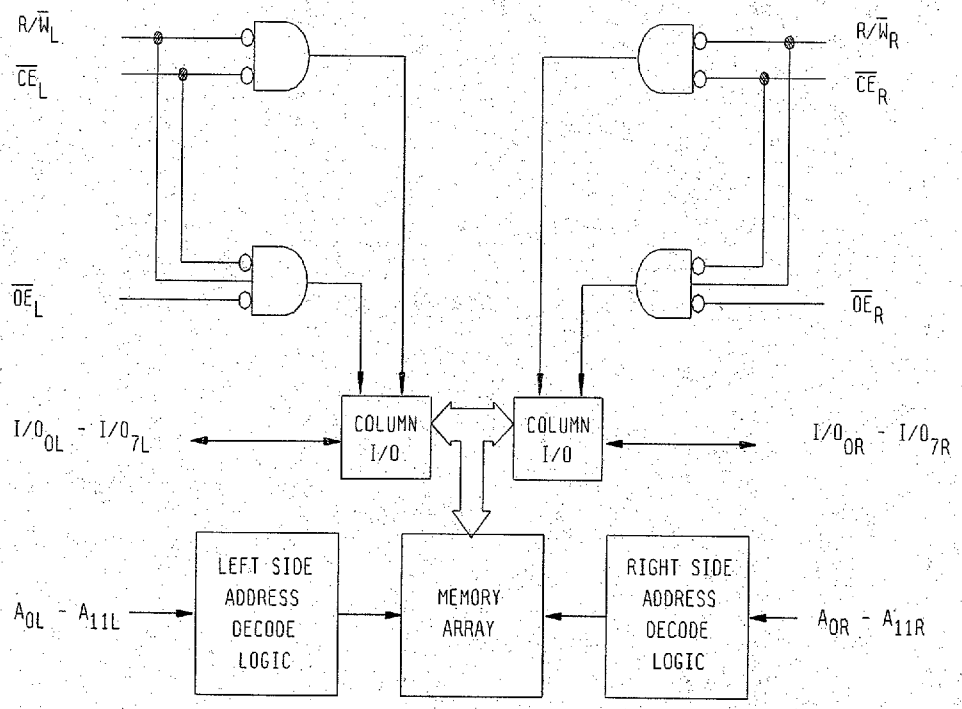
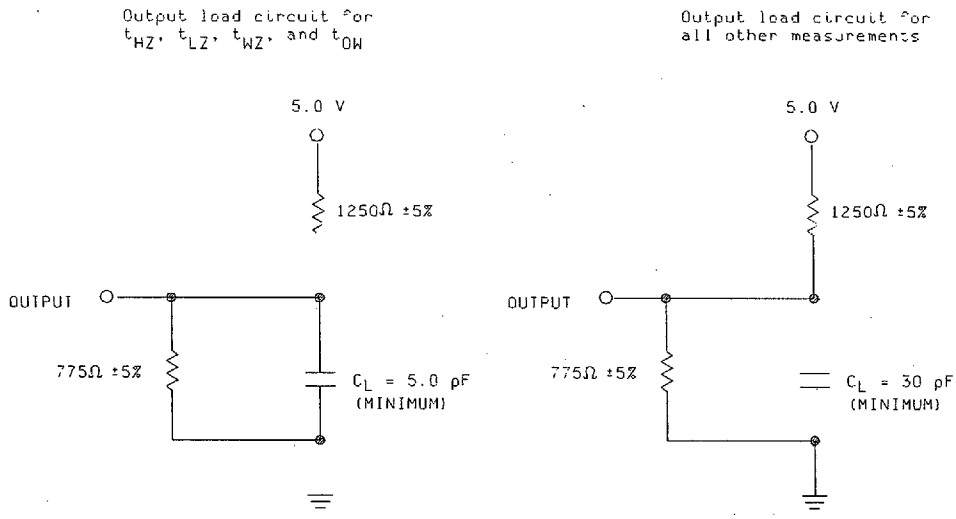


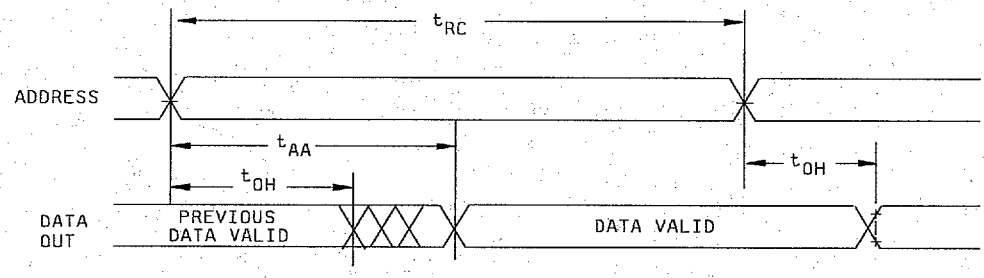
FIGURE 4. Functional block diagram.



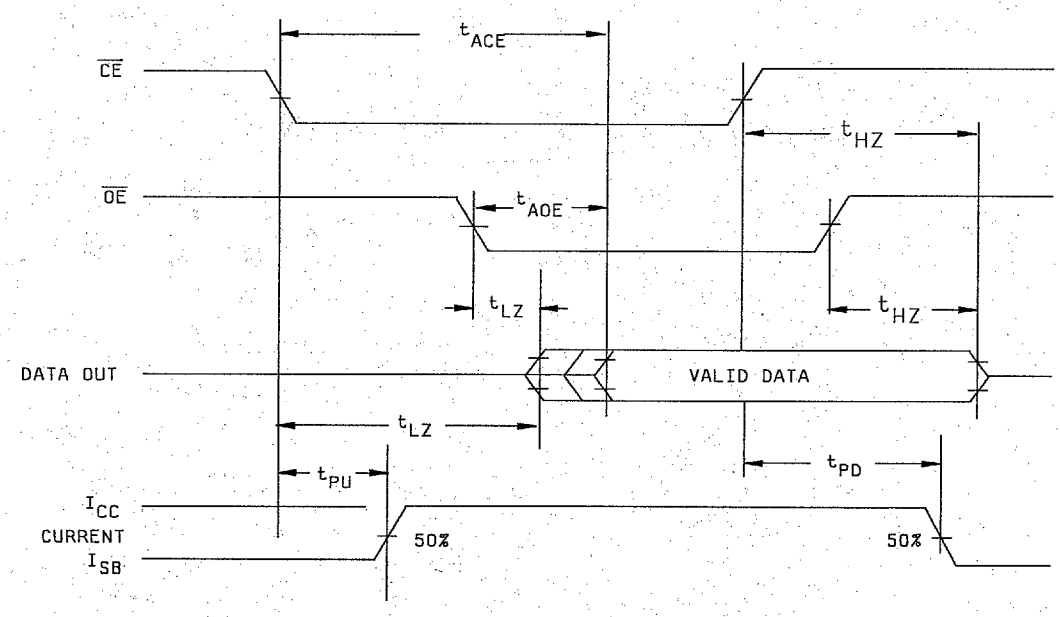
NOTES:
1. C_L = load capacitance and includes scope and jig capacitance.
2. Input pulse levels are at GND and 3.0 V.
3. Input rise and fall times are 5 ns.
4. Input timing reference levels are at 1.5 V.

FIGURE 5. Output load circuits.

Read cycle number 1, either side (see notes 1, 2, and 4)



Read cycle number 2, either side (see notes 1 and 3)



NOTES:
1. R/$\overline{W}$ is high for read cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

FIGURE 6. Timing waveform diagrams.

Write cycle number 1, R/$\overline{W}$ controlled (see notes 1, 2, 3, 4, 6 and 7)

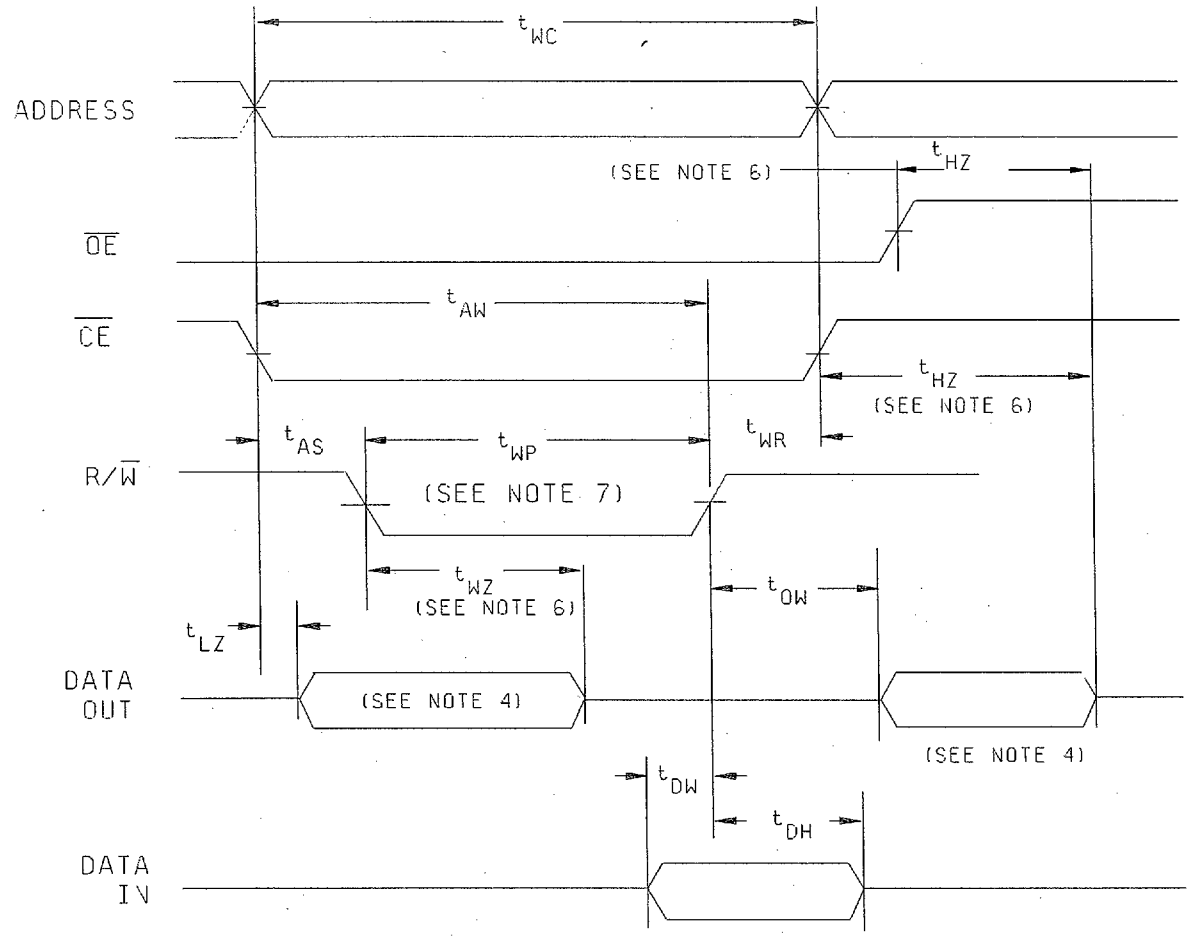


FIGURE 6. Timing waveform diagrams - Continued.

Write cycle 2, $\overline{CE}$ controlled (see notes 1, 2, 3, and 5)

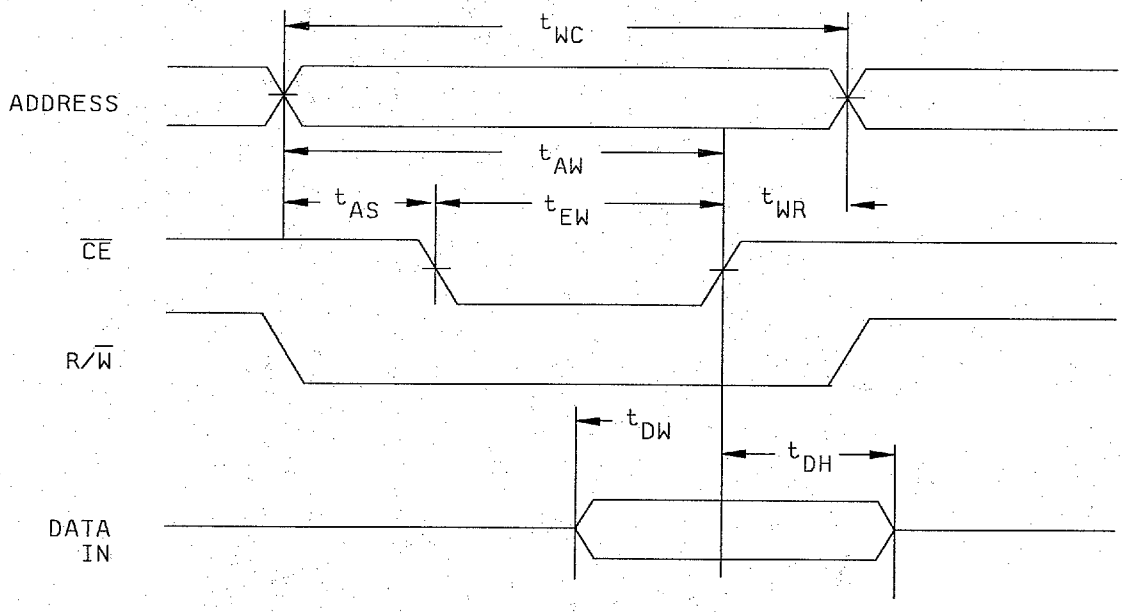
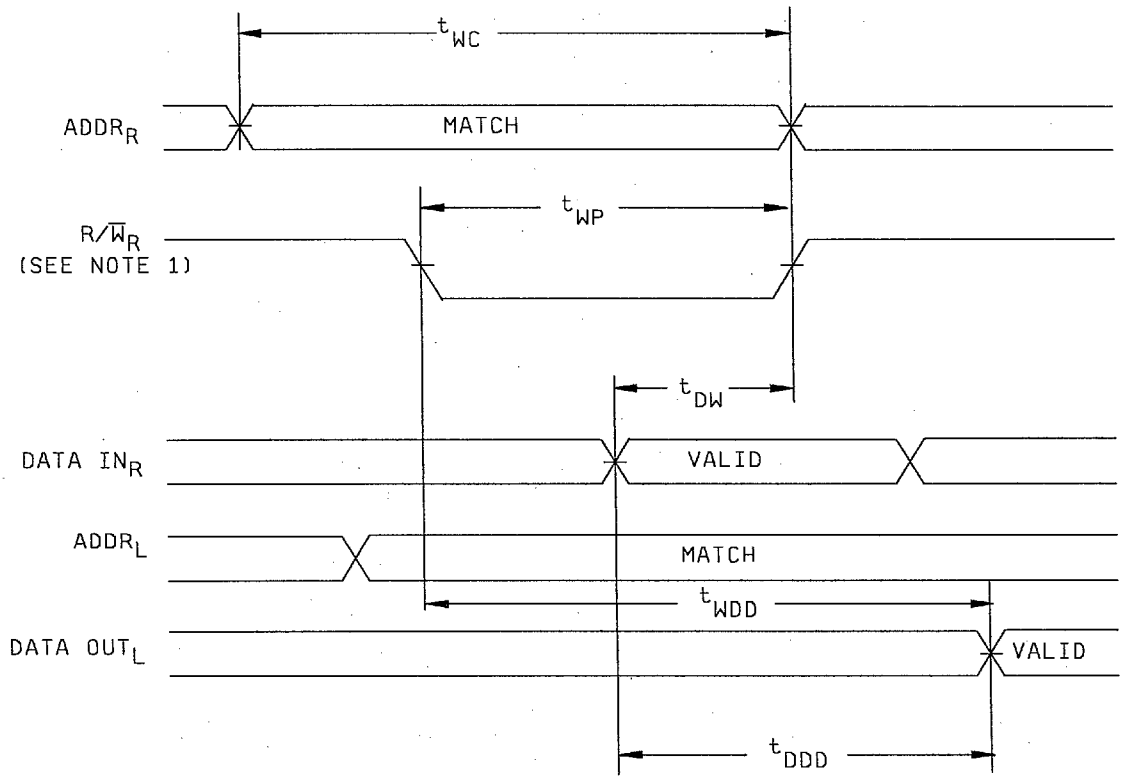


FIGURE 6. Timing waveform diagrams - Continued.

Timing waveform of read with port-to-port delay (see note 8)



NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500 mV from steady state with a 5.0 pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. Write cycle parameters should be adhered to in order to ensure proper writing.

FIGURE 6. Timing waveform diagrams - Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC2} Standby	±10 nA
I_{LI}, I_{LO}	±10 nA

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

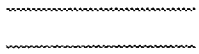
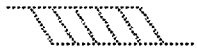
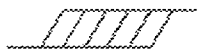
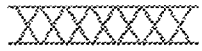
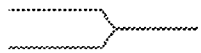
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

C_{IN}, C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{LI}	Input leakage current.
I_{LO}	Output leakage current.
T_C	Case temperature.
T_A	Ambient temperature,
V_{CC}	Positive supply voltage.
O/V	Latch-up over-voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (Data Retention Test).

30.1.1 Purpose. This test insures that the memory array will not lose data during a pause in operation as power remains applied to the device. Every memory cell must be checked to verify that it can retain both data states (1s and 0s). The manufacturer must determine the pause time required to allow sufficient time for defective memory cells to fail. Commom names for this type of algorithm include "Data Retention Test", "Static Hold Test", and "Stop Test".

30.1.2 Example Sequence.

Step 1. Write memory array to all 0"s.
Step 2. Pause for 100 milliseconds while VCC remains applied. No read or write operations are to occur during this period.
Step 3. Read memory array to verify data remains all 0"s.
Step 4. Write memory array to all 1"s.
Step 5. Pause for 100 milliseconds while V_{CC} remains applied. No read or write operations are to occur during this period.
Step 6. Read memory array to verify data remains all 1"s.

30.2 Algorithm B (Address Uniqueness Test).

30.2.1 Purpose. This test insures that each externally applied address corresponds to exactly one internal memory cell location. The algorithm is to detect all defects in the address decoders that result in multiple memory cells responding to a single address or result in some portion of the memory array becoming unaccessible to any address. Common algorithms that satisfy the requirement are "March Test", "XYMarch Test", and "Moving Inversion Test".

30.2.2 Example Sequence.

Step 1. Write memory array to all 0"s.
Step 2. Set target address to 0.
Step 3. Read target address, data should be 0.
Step 4. Write target address to 1.
Step 5. Increment target address and repeat steps 3 through 5 until all addresses have been the target address.
Step 6. Read entire array, data should be all 1s.
Step 7. Set target address to the maximum address in address space.
Step 8. Read target address, data should be 1.
Step 9. Write target address to 0.
Step 10. Decrement target address and repeat steps 8 through 10 until all addresses have been the target address.
Step 11. Read entire array, data should be all 0"s.

30.3 Algorithm C (Data Word Test).

30.3.1 Purpose. This test insures that each externally applied address corresponds to exactly one internal memory cell location. The algorithm is to detect all defects in the address decoders that result in multiple memory cells responding to a single address or result in some portion of the memory array becoming unaccessible to any address. Common algorithms that satisfy the requirement are "March Test", "XYMarch Test", and "Moving Inversion Test".

30.3.2 Example Sequence for x 8 device.

Step 1. Write data word "00000000" to address location 0.
Step 2. Write data word "11111111" to address location 1.
Step 3. Write data word "01010101" to address location 2.
Step 4. Write data word "10101010" to address location 3.
Step 5. Write data word "00110011" to address location 4.
Step 6. Write data word "11001100" to address location 5.
Step 7. Write data word "00001111" to address location 6.
Step 8. Write data word "11110000" to address location 7.
Step 9. Read data word "00000000" to address location 0.
Step 10. Read data word "11111111" to address location 1.
Step 11. Read data word "01010101" to address location 2.
Step 12. Read data word "10101010" to address location 3.
Step 13. Read data word "00110011" to address location 4.
Step 14. Read data word "11001100" to address location 5.
Step 15. Read data word "00001111" to address location 6.
Step 16. Read data word "11110000" to address location 7.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-10-23

Approved sources of supply for SMD 5962-89764 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8976401MXA	61772	IDT7134SA70CB
5962-8976401MYA	61772	IDT7134SA70L48B
5962-8976401MZA	61772	IDT7134SA70FB
5962-8976402MXA	61772	IDT7134LA70CB
5962-8976402MYA	61772	IDT7134LA70L48B
5962-8976402MZA	61772	IDT7134LA70FB
5962-8976403MXA	61772	IDT7134SA55CB
5962-8976403MYA	61772	IDT7134SA55L48B
5962-8976403MZA	61772	IDT7134SA55FB
5962-8976404MXA	61772	IDT7134LA55CB
5962-8976404MYA	61772	IDT7134LA55L48B
5962-8976404MZA	61772	IDT7134LA55FB
5962-8976405MXA	61772	IDT7134SA45CB
5962-8976405MYA	61772	IDT7134SA45L48B
5962-8976405MZA	61772	IDT7134SA45FB
5962-8976406MXA	61772	IDT7134LA45CB
5962-8976406MYA	61772	IDT7134LA45L48B
5962-8976406MZA	61772	IDT7134LA45FB
5962-8976407MXA	61772	IDT7134SA35CB
5962-8976407MYA	61772	IDT7134SA35L48B
5962-8976407MZA	61772	IDT7134SA35FB
5962-8976408MXA	61772	IDT7134LA35CB
5962-8976408MYA	61772	IDT7134LA35L48B
5962-8976408MZA	61772	IDT7134LA35FB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Inc. 2975 Stender Way Santa Clara, CA 95054

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.